MICROCYBER INC.

FBC0409 User Manual

Fieldbus Communication Controller
(According to IEC 61158)

Version: 1.2
Date: 06.08

Revision History

Version	Release Date	Detail of Changes
1.1	06.08.08	First release
1.2	07.03.16	Add Jabber Timer

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General Description

FBC0409 is a fieldbus interface and controller IC which conforms to IEC 61158 filedbus physical layer definition. It supports typical embedded CPU and MCU, and satisfies the demands of high performance fieldbus masters or slavers.

FBC0409 contains Manchester data encoder and decoder on chip. It requires a medium interface and external filter for connection to a fieldbus system, and can automatically correct bus polarity. FBC0409 also contains 4k bytes embedded data RAM, applying DMA controller. The implementation of message transmission and address resolution can be executed without CPU intervention. The Rx and Tx data status is available in status registers of FBC0409, such as status of line operation, code error, frame loss, frame collision.

FBC0409 implement a portion of data-link layer function. Tx/Rx frame check sequence (FCS), 16 bits 1ms timer, 16 bits 1/32ms timer, 16 bits octet time timer, frame code decoding and address resolution.

Features

FBC0409 is designed for fieldbus physical and part data link communication functions, details list below:

- Supports line data rate 31.25K Bit/S
- Build-in Manchester Encoder/Decoder
- Transmitter Jibber inhibit, receiver super long frame inhibit
- Automatic parity recognize and correct
- Message type and destination address detection automatically
- Automatic transmitter and receiver frame check
- Build-in three channels DMA controller， used to control data transmitting, receiving and address recognization looking up table memory management
- 4k bytes asynchronous SRAM internal as communication buffer for transmitting, receiving and address lookup table memory
- Length of Preamble, Start and Stop delimiter under software controlled
- Build-in bus arbiter, CPU accessing internal SRAM correctly
- Data link layer timer (1ms、1/32 ms、octet time timer)
- Designed lots of useful interrupt and status Registers
- Compatibility with INTEL、ARM serials CPU
- Internal loop back for test
- STANDBY feature
- Power supply: 2.7～5.5V
- Power consumption: <600uA

- Operating temperature range: -40℃～85℃
- Available in 44-pins TQFP package

Typical Application

Chip FBC0409 was designed as fieldbus communication controller, following is its typical application.

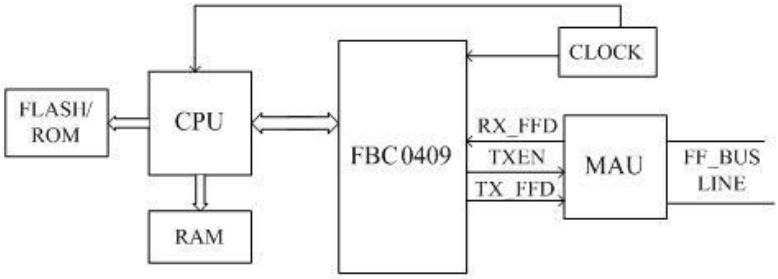

Figure 1　FBC0409 Controller Typical Application

Pin Assignment

FBC0409 is packaged in a 44-pins TQFP package，The body size is 10mm×10mm，pins pitch is 1.8mm.

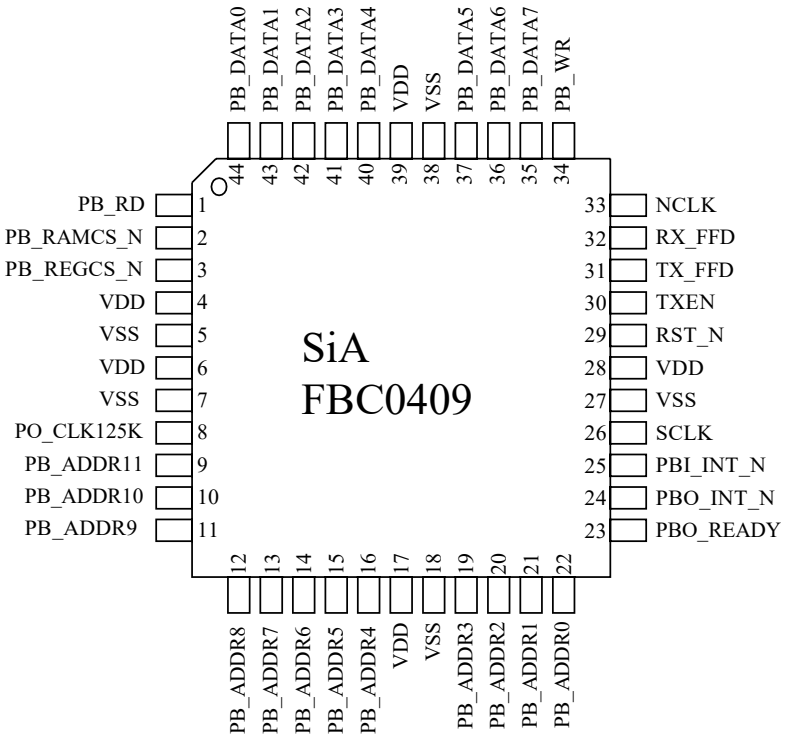

Figure 2　FBC0409 Pin Diagram

Table 1 FBC0409 Pin Description

NAME	TYPE	DEFINITION	NOTE
PB_ADDR[11:0]	INPUT	12 bits address bus	
PB_DATA[7:0]	INOUT	8 bits data bus	
PB_RAMCS_N	INPUT	internal SRAM selection, active low	
PB_REGCS_N	INPUT	Register chip select, active low	
RST_N	INPUT	system reset, active low	
PB_WR	INPUT	CPU write control	
PB_READY	INPUT	CPU read control	
SCLK	INPUT	system clock, same source as CPU	
NCLK	INPUT	line clock, independent of SCLK	
PO_CLK125K	OUTPUT	125k time clock output	
PO_RDY	OUTPUT	CPU delay request, PO_READY will active when CPU access internal SRAM which is busy	0 or HiZ
PBO_INT_N	OUTPUT	interrupt request to CPU, active low	
PBI_INT_N	INPUT	interrupt input from outside, active low	
TXEN	OUTPUT	fieldbus active indication, its level is decided by software	
TX_FFD	OUTPUT	fieldbus data output	
RX_FFD	INPUT	fieldbus bus data input	
VDD	POWER	power supply	
VSS	GND	ground	

Function Description

FBC0409 fieldbus controller conforms to IEC 61158 fieldbus physical layer definition, and supports typical embedded CPU and MCU, such as Intel 80188/80186 serials and ARM. FBC0409 meets the requirements of high performance fieldbus masters or slavers.

FBC0409 contains Manchester data encoder and decoder on chip. It requires only a medium interface and external filter for connection to a fieldbus system, and automatically correct line polarity. FBC0409 also contains 4k build-in 8 bits data RAM, applying DMA controller. Fieldbus data receiving, transmitting and received address looking up are done without CPU intervening. The Rx and Tx process status

is available in status registers of FBC0409, such as status of line operation, code error, frame loss, frame collision.

FBC0409 fieldbus controller implemeted parts functions of DLL. Tx/Rx frame check sequence (FCS), 16 bits 1MS timer, 16 bits 1/32MS timer, 16 bits octet timer, frame code decoding and address resolution. These data link functions are designed to reduce the CPU time.

FBC0409 contains a watchdog timer to avoid long time occupation on the fieldbus, while transmitting frame is longer than 512 bytes, the watchdog timer stops the transmitter. The built-in DMA controller manages three channels to access internal SRAM, it can enhance the network throughput. The SRAM is a 4k-8bits single port asynchronous SRAM, which is used for the storage of frames and address table. Figure 3 describes the internal block diagram of FBC0409.

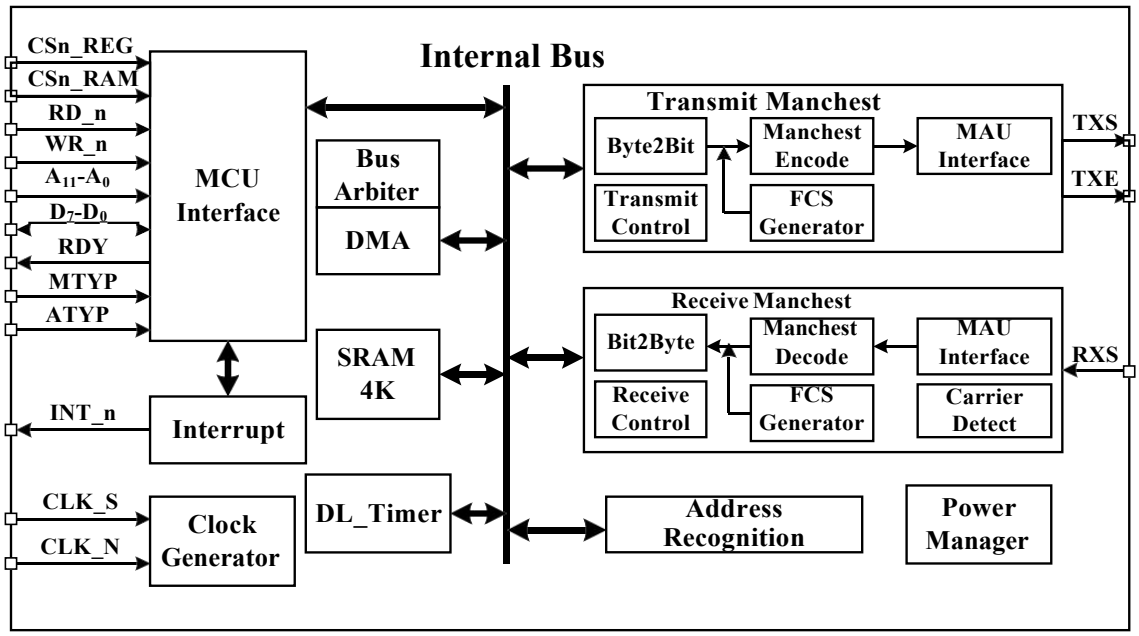

Figure 3 FBC0409 Internal Function Block Diagram

Note： The clock of bus arbiter and DMA/Interrupt controller is derived from SCLK, while in address recognization, bus data communication, timer, and the 500KHZ clock is divided clock of SCLK or NCLK.

1 CPU Interface

CPU interface block is bus interface between CPU and FBC0409, external CPU can access register and internal RAM of FBC0409 through CPU interface. Two addressing modes are supported, self addressing and share addressing. Decoding is

done in this block according to chip selection signal and address bus to generate signals to operate internal register and SRAM.

PO_READY is a handshake signal between CPU and FBC0409. While CPU accesses internal RAM and the RAM bus is under the control of internal function, PO_READY will be active for CPU to wait.

2 Register

FBC0409 is designed to receive configuration and command data from CPU or transmit internal data to CPU. CPU configures FBC0409 to operate correctly by accessing internal registers asynchronously in this module. CPU writes or reads internal registers by asserting PB_REGCS_N signal active (share chip selection signals), PB_WR active low when writes registers or PB_RD active low when reads registers.

3 Timer

Timer is a counter based on internal 500kHz clock, which is divided by SCLK or NCLK. Three timers are provided, 1 ms timer, 1/32 ms timer, octet time timer (256 us), to data link layer. All the three timers are 16 bits width and free running. They are all overflow to zero, accompanying a comparison value for each. Interrupts will be generated when anyone of the three timers overflow or reach comparison value. Note that before CPU reads any anyone of these timers, writes register 0x1F, which is used to latch timer value.

4 DMA Controller

DMA module is very important of FBC0409. All the communications are processed in this module after operation conditions configured. DMA controller contains three channels, receiving data storage (writing operation), transmitting data extraction (reading operation) and looking up address table (reading operation). The CPU tries to access SRAM while DMA controller is accessing it, bus arbiter module will set PO_READY with 0, the CPU is working on wait status.

5 Bus Arbiter

Bus arbiter locates between DMA module and host interface. It is used to switch between FBC0409 internal bus requests and external CPU bus requests to SRAM. DMA operation waits until current CPU access is finished. When DMA is operating, CPU tries to access RAM, PO_READY will be active at 0. When only DMA request

is active, PO_READY is not be set 0, DMA controls bus. When DMA request is not active, CPU controls bus.

6 Address Recognizing

This module is responsible for destination address filter and message mode. Address comparing enabled after ARME bit in command register is active, or else this module executes frame control word decoding only. Frame type information, such as frame control word, broadcast frame flag, PSA frame flag and frame code, will be obtained by frame decoding function. Additional, frame destination address type, node address, NS or HLNS address type will be obtained. Address match is performed according the type of destination address, if the address is node address, it is compared with NODE_ID[7:0] directly， and AMOF_INT is sent to CPU; if the incoming destination address is HL or NS type，which is compared with HL or NS address table in SRAM by DMA manner. If they are consistent, AMOF_INT or ETDF_INT is sent to CPU.

7 Bus Receiver

The function of the bus data receiver module focuses on receiving incoming data from fieldbus and abstracting data sections to higher layers, including clock and data recovery, delimiter detection, Manchester decoding, serial to parallel transforming, FCS checking, and generates corresponding data and status. This module is configured by CPU, that include receive data enable (RDE), full or half duplex mode (FDM) and loop back (LOOPBK) bits.

This module can be configured in two receive mode, DMA manner or CPU interrupt manner. In DMA manner (DRE is active), the received data is stored into internal SRAM directly and can be taken out after receiving finished. In CPU manner, the receive data full interrupt signal (RDRF_INT) will active after receive data register is full. The CPU responses interrupt by reading the register data. It is recommended to operate in DMA manner.

8 Bus Transmitter

This module transmits the data delivered by CPU to fieldbus. The data is disposed through adding preamble and delimiter, performing parallel to serial and Manchester encoding, adding frame check sequence. At the same time, it generates corresponding status and interrupt signals to CPU. CPU controls the operation of bus transmitter, including enable the module to work, preamble length configuration, transmitting frame CRC enable. Same as receiver, the transmitter also has two operation manners, DMA mode and CPU mode. When DMA enable (DTE) is active,

the transmitting data block is written into internal SRAM and data length has been configured before initialize transmitting by DMA controller. In CPU manner, initialize transmitter first, then nothing is done until transmit register empty interrupt signal (TDRE_INT) is active to request next byte to be transmitted. After all byte have been transmitted, transmitter stops. It is recommended to operate in DMA manner.

Note that transmit register (TRM_REG) must be executed an idle writing to start transmitting process. There are two mechanism to notify CPU to finish current transmitting, one is transmitting byte counter in transmitter is reach configure number, the other one is that the transmit register is not written more than one byte time. The length of the transmitting frame is longer than 512 bytes, the transmitting is fished by bus transmitter, at the same time, Jabber interrupt is active, and JI_INT signal is sent to CPU.

9 Clock Generator

This module generates the clocks for internal function blocks, including 500 KHz clock used in transmitter and receiver, fast clock used in DMA controller and bus arbiter. If clock mode is enabled (MD[1:0] ≠ 00), internal fast clock SCLK is decided by system clock divider CLK_DIV, the formula is SCLK/（CLK_DIV +1）. According to time constraints of internal asynchronous SRAM access, the generated clock must not be faster than 8MHz. If input clock is 32MHZ, thus the value of CLK_DIV should be more than 0x3; if input clock is 20MHZ, CLK_DIV should be more than 0x1. Note that divider must be one of 1/2/4/8/16 （CLK_DIV equal to 0/1/3/7/15）.The 500KHz clock is decided by SCLK, NCLK and command register 2. CLKSEL selects source clock, 0 is SCLK, 1 is NCLK, then divided by BR [4:0] to obtain 500KHz clock.

MD definition： 00:
clock stops,
01: H1 bit rate, it is no effect of other value.
BR definition：CLK500 = ICLK/(BR+1), BR is one of 0/1/3/7/15/31.

10 Interrupt Function

This module generates interrupt signals according to internal status signals, and executes interrupt clearing, interrupt masking. Note that when 1 is written to the corresponding bit of interrupt address, the interrupt will be cleaned. Masking interrupt also clears it, and the interrupt bit will never set until the mask bit convert to 1. Note that the interrupt cleaning operation is executed on interrupt address.

Address Mapping

The address space of FBC0409 divided into two parts, register area and 4k SRAM area, depending on addressing mode and MSB of address bus. Two methods of addressing are supported by chip selection signals. One is that only one chip select signal is connected to both pins of REG_CSN and RAM_CSN, another one is that pin REG_CSN connects to pin CS1_n of CPU and pin RAM_CSN connects to pin CS2_n of CPU. Here we call the former method 1 and the latter method 2.

In method 2, separate address corresponds to register space and SRAM space. In this manner, address decoding performs independently according to chip selection signals. When the chip selection signal of register is active, the chip selection signal of SRAM is deserted, the address of register is between 0x00 and 0x3F. When the chip selection signal of SRAM is active, the chip selection signal of register is deserted, the address of SRAM is between 0x000 and 0xFFF.

In method 1, address space is shared both register area and SRAM area. Register space is between 0xFC0 and 0xFFF, SRAM space is between 0x000 and 0xFBF.

FBC0409 Register

Table 2 FBC0409 Register

Offset	Name	Description	Attribute	Note
0x00	TRM_REG[7:0]	Transmit data register	WO	DATA REG
	RCV_REG[7:0]	Receive data register	RO	
0x01	FB_CMD0[5:0]		W/R	CMD REG
	PSE[1:0]	Bit[1:0] Preamble length		
	TFCE	Bit[2] Transmit FCS enable		
	TDE	Bit[3] Transmit data enable		
	FDM	Bit[4] Duplex enable		
	RDE	Bit[5] Rx data enable		
0x02	FB_CMD1[4:0]		W/R	CMD REG
	ARME	Bit[0] Address recognize mode enable		

	DRE	Bit[1] DMA Rx enable		
	DTE	Bit[2] DMA Tx enable		
	LOOPBK	Bit[3] Loop back control		
	MAU_ENF	Bit[4] MAU Tx enable flag		
0x03	FB_CMD2[7:0]		WO	CMD REG
	BR[4:0]	Bit[4:0] Clock division scale, obtain 500K clock		
	MD[1:0]	Bit[6:5] Time mode, 00：silent		
	CLKSEL	Bit[7] Clock select control		
0x03	ISR_MSTR[4:0]		RO	INTERRUPT MASTER
	CISF	Bit[0] Indicates communication interruption		
	AISF	Bit[1] Indicates address recognize interruption		
	TISF	Bit[2] Indicates TIMER/ CLOCK interruption		
	ERRF	Bit[3] Indicates error		
	EIF	Bit[7] PI_INT interruption		
0x04	ISR0[7:0]		RC	INT0
	TDRE_INT	Bit[0] Tx register blank		
	TIF_INT	Bit[1] Data tx finish		
	RIF_INT	Bit[2] Data rx finish		
	REDF_INT	Bit[3] Receive end delimiter		
	REF_INT	Bit[4] Rx register overflow		
	RSDF_INT	Bit[5] Receive start delimiter		

	RAF_INT	Bit[6] Fieldbus active		
	RDRF_INT	Bit[7] Rx register full		
0x04	INT_CLR0[7:0]	Writing 1 to clear corresponding interruption	WO	CLEAR INT0
0x05	ISR1[3:0]		RC	INT1
	BMDF_INT	Bit[0] Rx broadcast		
	AMDF_INT	Bit[1] Rx address match		
	EOTF_INT	Bit[2] Address table look up finish		
	FCF_INT	Bit[3] Recognize address code		
0x05	INT_CLR1[3:0]	Writing 1 to clear corresponding interruption	WO	CLEAR INT1
0x06	ISR2[5:0]		RC	INT2
	MS1_32COF_INT	Bit[0] 1/32ms timer overflow		
	MS1_32CF_INT	Bit[1] 1/32ms timer reach to compare value		
	MS1COF_INT	Bit[2] 1ms timer overflow		
	MS1CF_INT	Bit[3] 1ms timer reach to compare value		
	OOF_INT	Bit[4] Timer overflow		
	OCF_INT	Bit[5] Timer reach to compare value		
0x06	INT_CLR2[5:0]	Writing 1 to clear corresponding interruption	WO	CLEAR INT2
0x07	ISR3[6:0]		RC	INT3
	LSDF_INT	Bit[0] Rx start delimiter		
	LEDF_INT	Bit[1] Rx end delimiter		
	LNGFRM_INT	Bit[2] Rx long frame		

	MDERR_INT	Bit[3] Rx Manchester code		
	LCD_INT	Bit[4] Loss CD when receiving		
	TRM_FAIL_INT	Bit[5] Transmit failure		
	JI_INT	Bit[6] Jibber indication		
0x07	INT_CLR3[6:0]	Clean corresponding interrupt by writing 1	WO	CLEAR INT3
0x08	ISR0_MSK[7:0]	Mask of ISR0	W/R	
0x09	ISR1_MSK[3:0]	Mask of ISR1	W/R	
0x0A	ISR2_MSK[5:0]	Mask of ISR2	W/R	
0x0B	ISR3_MSK[6:0]	Mask of ISR3	W/R	
0x0C	TRM_BYTECNT[13:8]	MSB of Tx bytes counter	W/R	
0x0D	TRM_BYTECNT[7:0]	LSB of Tx bytes counter	W/R	
0x0E	TRM_BUFPTR[13:8]	MSB of tx data buffer pointer when in DMA mode	W/R	
0x0F	TRM_BUFPTR[7:0]	LSB of tx data buffer pointer when in DMA mode	W/R	
0x10	reserved	used in the future		
0x11	reserved	used in the future		
0x12	RCV_BUFPTR[13:8]	MSB of Rx data buffer pointer when in DMA mode	W/R	
0x13	RCV_BUFPTR[7:0]	LSB of Rx data buffer pointer when in DMA mode	W/R	
0x14	reserved	used in the future		
0x15	reserved	used in the future		
0x16	MATCH_VECT[13:8]	MSB of address match vector	RO	
0x17	MATCH_VECT[7:0]	LSB of address match vector	RO	
0x16	ADR_TABNS[13:8]	MSB of NS table pointer	WO	
0x17	ADR_TABNS[7:0]	LSB of NS table pointer	WO	
0x18	FRAME_CODE[4:0]	Frame code received	RO	

0x19	FRAME_CONTRL[7:0]	Frame control code received	RO	
0x18	ADR_TABHLNS[13:8]	MSB of HLNS table pointer	WO	CONFIGURE
0x19	ADR_TABHLNS[7:0]	LSB of HLNS table pointer	WO	CONFIGURE
0x1A	reserved	used in the future		
0x1B	NODE_ID[7:0]	Node identifier address	W/R	CONFIGURE
0x1C	STATUS0[7:0]		RO	STATUS0
	TDRE_STAT	Bit[0] Tx register blank		
	TIF_STAT	Bit[1] Data Tx finish		
	FCSF_STAT	Bit[2] FCS correct		
	REDF_STAT	Bit[3] Receive data end delimiter		
	RDEF_STAT	Bit[4] Receive buffer overflow		
	RSDF_ STAT	Bit[5] Receive data start delimiter		
	RAF_ STAT	Bit[6] Fieldbus active		
	RDRF_STAT	Bit[7] Rx register is full		
0x1D	STATUS1[7:0]		RO	STATUS1
	RBMF_STAT	Bit[0] Broadcast address recognized		
	AMOF_STAT	Bit[1] Address match flag		
	ETDF_STAT	Bit[2] Table lookup end		
	RFCF_STAT	Bit[3] Frame control code received		
	RPSAF_STAT	Bit[4] PSA frame received		
	RNAF_STAT	Bit[5] Node address received (8bits)		

	NS_STAT	Bit[6] NS address request(16bits)		
	HL_STAT	Bit[7] HL address request (32bits address)		
0x1E	STATUS2[6:0]		RO	STATUS2
	LSDF_STAT	Bit[0] Loss of start delimiter error		
	LEDF_STAT	Bit[1] Loss of end delimiter		
	LNGFRM_STAT	Bit[2] Long frame received		
	MDERR_STAT	Bit[3] Manchester code error		
	LCD_STAT	Bit[4] Loss carrier when receiving		
	LTAF_STAT	Bit[6] Address table lookup requesting		
	RSPF_STAT	Bit[7] Disparity indication		
0x1F	TIMER_LATCH	Latch timer control, active when write 0xff		
0x20	MS1_32CNT[15:8]	1/32ms timer MSB	RO	
0x21	MS1_32CNT[7:0]	1/32ms timer LSB	RO	
0x20	MS1_32COMP[15:8]	1/32ms compare value MSB	WO	
0x21	MS1_32COMP[7:0]	1/32ms compare value LSB	WO	
0x22	MS1_CNT[15:8]	1ms timer MSB	RO	
0x23	MS1_CNT[7:0]	1ms timer LSB	RO	
0x22	MS1_COMP[15:8]	1ms comppare value MSB	WO	
0x23	MS1_COMP[7:0]	1ms compare value LSB	WO	
0x24	OCT_CNT[15:8]	Octet timer MSB	RO	
0x25	OCT_CNT[7:0]	Octet timer LSB	RO	
0x24	OCT_COMP [15:8]	Octet compare value MSB	WO	

0x25	OCT_COMP [7:0]	Octet compare value LSB	WO	
0x26	CLK_DIV [3:0]	RAM write/read pulse width control	W/R	
0x27	test	Fix value of 0x01	W/R	

Registers are divided into eight groups according to their different functions：Transmitting Registers, Receiving Registers, Command Registers, Interruption Registers, DMA control Registers, Address recognition Registers and Timer registers, as show as below.

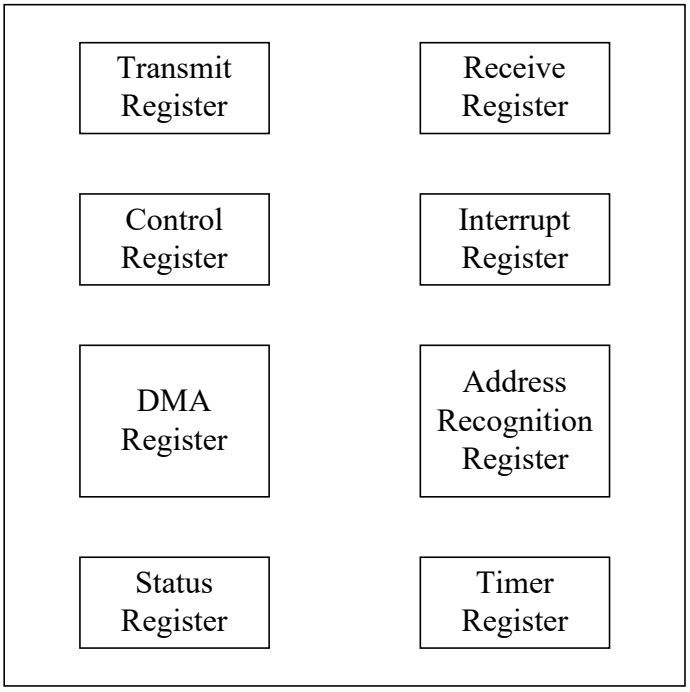

Figure 4 FBC0409 Internal Register Group

Transmit Data Register (TRM_REG): Address 0x00

FBC0409 is designated two modes sending data to fieldbus, which are CPU manner and DMA manner. CPU transmits data directly through writing transmit data register which address is 0x00. In order to avoid transmit data overflow and prepare transmit module. CPU should read the status bit of TDRE (Status Regiter0, address 0x1C, bit[0]) or interrupt status TDRE_INT (Interrupt Status Register0,adderss 0x04, bit [0]). First, if TDRE or TDRE_INT is true， which indicates that the transmit data register is empty. New data should be written and clear the current interrupt to wait for next byte to transmit. All steps above are automatically performed in DMA manner when transmit data has been stored in Tx buffer and transmit has been initialized.

Additional, initialization is done by writing transmit data register in all two mentioned manners. When an idle state is written in the transmit data register, the first operation is starting the transmittion, the data should be ignored, the valid data follows. And, it is no effects to write transmit data register in DMA mode.

Receive Data Register(RCV_REG): Address 0x00

The receive data register stores data received from fieldbus and is accessed by CPU when reading address 0x00. Similarly to transmit data register, in order to avoid this register under run (cause frame error) or overflow (loss of frame data), CPU should read status register RDRF（Status Register0，address 0x1C, bit [1]） or interrupt status register RDRF_INT（Interrupt Status Register，address 0x04,bit [1]）. And if RDRF or RDRF_INT is true， which indicates that one new byte data has been received, CPU read the data immediately. In the DMA manner, all the steps automatically performed, the received data is store in the SRAM on chip.

COMMAND REGISTERS

Command registers decide FBC0409 operation configuration and common control, including three command registers. Here is detail.

Command Register 0 (FB_CMD): Address 0x01

0	0	RDE	FDM	TDE	TFCE	PSE[1:0]

RDE (RECEIVE DATA ENABLE): Fieldbus data receive control,

0: disable receive, 1: enable receive.

FDM (FULL/HALF DUPLEX MODE): Full duplex/half duplex mode selection,
0: half duplex, 1: full duplex.

TDE (TRANSMIT DATA ENABLE): Fieldbus data transmit control,
0: disable transmit, 1: enable transmit.

TFCE (TRANSMIT FRAME CHECK ENABLE): Transmit FCS enable,
0: disable FCS, 1: enable FCS.

PSE[1:0] (PREAMBLE SEQUENCE ENABLE): Preamble length configure,
00B: 1byte, 01B: 2 bytes, 10B: 3 bytes, 11B: 4 bytes.

Command Register 1 (FB_CMD1): Address 0x02

0	0	0	MAU_ENF	LOOPBK	DTE	DRE	ARME

MAU_ENF (MAU ENABLE FLAG): MAU enable flag，transmit enable to MAU is high level when transmit active setting this bit to 1, otherwise, set this bit to 0.

LOOPBK (LOOPBACK MODE FLAG): Internal loop back control, transmit will internal loop back when set this bit to 1.

DTE (DMA TRANSMIT ENABLE): DMA transmit enable control,
0: disable DMA transmit, 1: enable DMA transmit.

DRE (DMA RECEIVE ENABLE): Enable DMA receive,
0: disable DMA receive, 1: enable DMA receive.

ARME (ADDRESS RECOGNITION MODE ENABLE): Enable address recognize mode,
0: disable, 1: enable.

Command Register 2 (FB_CMD2)：Address 0x03

CLKSEL	MD1	MD0	BR4	BR3	BR2	BR1	BR0

CLKSEL (CLOCK SOURCE SELECTS): Line clock source selects,

0: CPU clock SCLK, 1: NCLK.

MD[1:0] (CLOCK MODE SELECTS): Disable internal clock when is set to 11B, otherwise configure fieldbus communication rate 31.25kbps.

BR[4:0] (BAUD RATE SELECT): Divider to get the internal 500kHz clock used the clock select by CLKSEL, formula: Input Clock/（BR+1）. E.g. Input Clock is 16MHZ， thus BR[4:0] should be 0x1F. This value only supports 1/2/4/8/16/32 division, corresponding BR is 0/1/3/7/15/31.

Command Register 3(FB_CMD3): Address 0x26

0	0	0	0	CLK_DIV[3:0]

CLK_DIV[3:0] (INTERNAL CLOCK DIVIDER): It get 4~6M clock by divides SCLK using SCLK/（CLK_DIV +1）. E.g. if input clock is 32MHz, thus the value of CLK_DIV should be 0x7; if input clock is 20MHZ, thus CLK_DIV should be 0x3. Only 1/2/4/8/16 supported , (CLK_DIV is 0/1/3/7/15).

INTERRAUPT REGISTERS

Several interrupt provided on FBC0409, including Interrupt Index Register, Interrupt Status Register0-3, Interrupt Mask Regiter0-3.

Interrupt Index Register (ISR_MSTR): Address 0x03

Interrupt index register indicates the source of interrupt

EIF	0	0	0	ERRF	TISF	AISF	CISF

EIF (EXTERNAL INTERRUPT FLAG): Outside interrupt indication， active when PI_INT = 0.

ERRF (ERROR CAUSED BY INTERRUPT): Any bit in ISR3 is high then this bit is active high.

TISF (TIMER INTERRUPT SOURCE FLAG): Any bit of six in ISR2 is high then this bit is active high.

AISF (ADDRESS INTERRUPT SOURCE FLAG): Any bit of four in ISR1 is high then this bit is active high.

CISF (COMMUNICATION INTERRUPT SOURCE FLAG): Any bit of eight in ISR0 is high then this bit is active high.

Note：Any bit of four in ISR_MSTR is 1, output pin PO_INT is active low.

Interrupt Status Register 0 (ISR0): Address 0x04

Interrupt status register0 stores the interrupts generated in communication process and are cleaned by writing 1 to corresponding bit at the same address.

RDRF_INT	RAF_INT	RSDF_INT	REF_INT	REDF_INT	RIF_INT	TIF_INT	TDRE_INT

RDRF_INT (RECEIVE DATA REGISTER FULL): RDRF_INT is active high when receive module has received one whole byte.

RAF_INT (RECEIVE ACTIVE FLAG): RAF_INT is active high when detects the CD signal on line.

RSDF_INT (RECEIVE START DELIMITER FLAG): RSDF_INT is active high when start delimiter is detected.

REF_INT (RECEIVE ERROR FLAG): REF_INT is active high when receive data register overflows.

REDF_INT (RECEIVE END DELIMITER FLAG): REDF_INT is active high after detecting frame end delimiter, it also indicates the current receive finished.

RIF_INT (RECEIVE IDLE FLAG): RIF_INT is active high after frame receives finish.

TIF_INT (TRANSMIT IDLE FLAG): TIF_INT is active high after frame transmits

finish, and indicates another frame can be initialized.

TDRE_INT (TRANSMIT DATA REGISTER EMPTY): TDRE_INT is active high when transmit module requests a new byte to transmit

Interrupt Status Register 1 (ISR1): Address 0x05

Interrupt status register1 stores interrupt status caused in address recognize processes and are cleaned by writing 1 to corresponding bit at the same address.

0	0	0	0	FCF_INT	EOTF_ING	AMDF_INT	BMDF_INT

FCF_INT (FRAME CONTROL FLAG): FCF_INT is active high when frame control word is received in address recognize module.

EOTF_INT (END OF TABLE FLAG): ETOF_INT is active high when lookup table gets to the end（continuous 0 address）.

AMDF_INT (ADDRESS MATCH DETECTION FLAG): AMDF_INT is active high when address matches.

BMDF_INT (BROADCAST MESSAGE DETECTION FLAG): BMDF_INT is active high when current receiving frame is a broadcast frame.

Interrupt Status Register 2 (ISR2): Address 0x06

Interrupt status register2 stores interrupt status caused in timer module and are cleaned by writing 1 to corresponding bit at the same address.

0	0	OCF	OOF	1CF	1OF	1/32CF	1/32OF

OCF (OCTET COUNTER FLAG): Octet timer gets to compare value interrupt. OCF is active high.

Note: The timer and the compare value are all 0 when RESET, this bit will active after reset, clean it before use.

OOF (OCTET OVERFLOW FLAG): Octet timer overflow interrupt indication (get to 0xFFFF), OOF is active high.

1CF (1MS COUNTER FLAG.): 1MS timer gets to its compare value, same as OCF.

1OF (1MS OVERFLOW FLAG): 1MS timer overflow interrupt indication, same as OOF.

1/32CF (1/32MS COUNTER FLAG): 1/32MS timer gets to compare value, same as OCF.

1/32OF (1/32MS OVERFLOW FLAG): 1/32MS overflow interrupt indication, same as OOF.

Interrupt Status Register 3 (ISR3): Address 0x07

Interrupt status register3 stores interrupt caused by error status and are cleaned by writing 1 to corresponding bit at the same address.

0	JI_INT	TRM_FAIL_INT	LCD_INT	LNGFRM_INT	MDERR_INT	LEDF_INT	LSDF_INT

JI_INT (JABBER INDICATION): Active high when jibber happened.

TRM_FAI_INT (TRANSMIT FAILUE): Active high when transmit was initialized without data.

LCD_INT (LOST CARRIER DETECTION): Active high when loss of carrier in receiving process.

LNGFRM_INT (LONG FRAME): Active high when long frame input error interrupt.

MDERR_INT (MANCHESTER DECODE ERROR): Active high when code error in input manchester code stream.

LEDF_INT (LOST END DELIMITER FLAG): Active high when loss of frame end delimiter in receiving process.

LSDF_INT (LOST START DELIMITER FLAG): Active high when loss of start delimiter in receiving process.

Interrupt 0 Mask Register (ISR0_MSK): Address 0x08

Interrupt mask register0 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Interrupt 1 Mask Register (ISR1_MSK): Address 0x09

Interrupt mask register1 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Interrupt 2 Mask Register (ISR2_MSK): Address 0x0A

Interrupt mask register2 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

Interrupt 3 Mask Register (ISR3_MSK): Address 0x0B

Interrupt mask register3 is used to disable or enable corresponding interrupt bit. Interrupt bit is enabled by setting mask bit to 1, otherwise clear it.

CONFIGURE REGISTERS

Transmit Bytes Counter Register (TRM_BYTECNT[13:0]):
Address 0x0C-0x0D

Transmit byte number configure in DAM mode. Write MSB first, followed by LSB immediately when change the configuration.

Transmit Buffer Pointer Register (TRM_BUFPTR[13:0]): Address 0x0E-0x0F

Transmit buffer pointer in DMA mode. Write MSB first, followed by LSB immediately when change the Register.

Receive Buffer Pointer Register (RCV_BUFPTR[13:0]): Address 0x12-0x13

Receive data buffer pointer, points to current frame storage start address in SRAM in DMA mode, and indicates the current frame end address minus 1. Write MSB first, followed by LSB immediately when change the Register.

Address Match Vector Register (MATCH_VECTOR[13:0]: Address 0x16-0x17

Points to the next address after operation of address recognization whenever match or not. Read only.

NS Address Table Pointer Register (ADR_TABNS[13:0]): Address 0x16-0x17

The start address of NS address-table in SRAM， Write only. Write MSB first, followed by LSB immediately when changing the Register.

Frame Control Word Register (FRAME_CNTRL[7:0]): Address 0x18

Store the frame control word in received fieldbus data, read only.

Frame Code Register (RAME_CODE[4:0]): Address 0x19

Stores the decode information of frame control word, 5 bits. CPU can access it after frame control word indication is active. Encoding rules lists in table 3.

Table 3 Frame Code/Frame Type Table

FCODE	MESSAGE FUNCTION	FCODE	MESSAGE FUNCTION
00000	ESTABLISH CONNECTION 1	10000	DATA TRANSFER 5
00001	ESTABLISH CONNECTION 2	10001	STATUS RESPONSE
00010	DISCONNECT CONNECTION 1	10010	COMPEL TIME
00011	DISCONNECT CONNECTION 2	10011	TIME DISTRIBUTION
00100	RESET CONNECTION 1	10100	ROUND-TRIP QUERY
00101	RESET CONNECTION 2	10101	ROUND-TRIP REPLY
00110	COMPEL ACKNOWLEDGE 1	10110	PROBE NODE
00111	COMPEL ACKNOWLEDGE 2	10111	PROBE RESPONSE
01000	COMPEL DATA 1	11000	PASS TOKEN

01001	COMPEL DATA 2	11001	EXECUTE SEQUENCE
01010	EXCHANGE DATA 1	11010	RETURN TOKEN
01011	EXCHANGE DATA 2	11011	REQUEST INTERVAL
01100	DATA TRANSFER 1	11100	CLAIM LAS
01101	DATA TRANSFER 2	11101	TRANSFER LAS
01110	DATA TRANSFER 3	11110	WAKE UP
01111	DATA TRANSFER 4	11111	IDLE

HLNS Address Table Pointer Register (ADR_TABHLNS[13:0]):
Address 0x18-0x19
The start address of HLNS address lookup table in SRAM， Write only. Write MSB first, followed by LSB immediately when changing the Register. If input frame is of HLNS type address, this table is used to match destination address.

Node Identifier Register (NODE_ID): Address 0x1B
Store 8 bits node identifier.

STATUS REGISTERS
Status Register 0 (STATUS0): Address 0x1C
Status register0 stores the status information in communication process. Read only.

RDRF_STAT	RAF_STAT	RSDF_STAT	REF_STAT	REDF_STAT	FCSF_STAT	TIF_STAT	TDRE_STAT

RDRF_STAT (RECEIVE DATA REGISTER FULL): RDRF_STAT is active high when receive module has received one whole byte.

RAF_STAT (RECEIVE ACTIVE FLAG): RAF_STAT is active high when detects the CD signal on line.

RSDF_STAT (RECEIVE START DELIMITER FLAG): RSDF_STAT is active high when start delimiter is detected.

REF_STAT (RECEIVE ERROR FLAG): REF_STAT is active high when receive data register overflows.

REDF_STAT (RECEIVE END DELIMITER FLAG): REDF_STAT is active high after detects frame end delimiter; it also indicates the current receive finished.

FCSF_STAT (FRAME CHECK SEQUENCE FLAG): RIF_STAT is active high when Rx FCS is error.
TIF_STAT (TRANSMIT IDLE FLAG): TIF_STAT is active high after frame transmits finish, and indicates another frame can be initialized.

TDRE_STAT (TRANSMIT DATA REGISTER EMPTY): TDRE_STAT is active high when transmit module request new byte to transmit.

Status Register 1 (STATUS1): Address 0x1D

Status register1 stores the status information in address recognition process. Read only.

HL_STAT	NS_STAT	RNAF_STAT	RPSAF_STAT	RFCF_STAT	ETDF_STAT	AMOF_STAT	RBMF_STAT

HL_STAT (HIGH LINK FLAG): HLNS_STAT is active high when HL address frame received.

NS_STAT (NODE SELECT FLAG): NS_STAT is active high when NS address frame received.

RNAF_STAT (RECEIVE NODE ADDRESS FLAG): RNAF_STAT is active high when NODE ID address frame received.

RPSAF_STAT (RECEIVE PSA FLAG): RPSAF_STAT is active high when PSA frame received.

RFCF_STAT (RECEIVE FRAME CONTROL FLAG): FCF_STAT is active high when frame control word is received in address recognize module.

ETDF_STAT (END OF TABLE DETECTION FLAG): ETOF_STAT is active high when lookup table get to the end（continuous 0 address）.

AMOF_STAT (ADDRESS MATCH OCCURENCE FLAG): AMDF_STAT is active high when address matches.

RBMF_STAT (RECEIVE BROADCAST MESSAGE FLAG): BMDF_STAT is active high when Current receiving frame is a broadcast frame.

Status Register 2 (STATUS2): Address 0x1E

Status register2 stores the error status information. Read only.

RSPF_STAT	LTAF_STAT	0	LCD_STAT	MDERR_STAT	LNGFRM_STAT	LEDF_STAT	LSDF_STAT

RSPF_STAT (REVERSED SIGNAL POLARITY FLAG): Disparity indication.

LTAF_STAT (LOOKUP TABLE ACTIVITY FLAG): Address table lookup is in process。

LCD_STAT (LOST CARRIER DETECTION): LCD_STAT is active high when loss of carrier in processing of receives.

LNGFRM_STAT (LONG FRAME): LNGFRM_STAT is active high when long frame input error happened.

MDERR_STAT (MANCHESTER DECODE ERROR): MDERR_STAT is active high when code error in input Manchester code stream.

LEDF_STAT (LOST END DELIMITER FLAG): LEDF_STAT is active high when loss of frame end delimiter in receiving processes.

LSDF_STAT (LOST START DELIMITER FLAG): LSDF_STAT is active high when loss of start delimiter in receiving processes.

TIMER REGISTERS

Timer Registers Latch Control (TIMER_LATCH): Address 0x1F

Issue writing operation of this register first before get the internal timer, used to latch internal timer.

1/32MS Timer Register (MS1_32CNT[15:0]: Address 0x20-0x21

1/32MS timer register, read only.

1/32MS Timer Comp Value (MS1_32COMP[15:0]): Address 0x20-0x21

1/32MS timer comparison value, write only.

1MS Timer Register (MS1_CNT[15:0]): Address 0x22-0x23

1MS timer register, read only.

1MS Timer Comp Value (MS1_COMP[15:0]): Address 0x22-0x23

1MS timer comparison value, write only.

Octet Timer Register (OCTET_CNT[15:0]): Address 0x24-0x25

Octet timer register, read only.

Octet Timer Comp Value (TET_COMP[15:0]): Address 0x24-0x25

Octet timer comparison value, write only.

Characteristics

1 Thermal Information

- Storage temperature：-65~150℃；
- Operating temperature：-40~85℃；
- Long-term operating junction temperature：-40~85℃

2 DC/AC Characteristics

Table 4　FBC0409 DC_1. Characteristics

Parameter	Symbol	VDD=3.3V±10% −40℃≤Ta≤85℃	Min.	Typical	Max.	Units
Input Voltage, High	V_{IH}	(1)	2.2	-	-	V
		(2)	1.3	1.8	2.3	
Input Voltage, Low	V_{IL}	(1)	-	-	1	V
		(2)	0.9	1.2	1.4	
Output Voltage, Low	V_{OL}	I_{OL} = 1.8mA	-	-	0.4	V
		I_{OL} = 9mA	-	-	1	
Output Voltage, High	V_{OH}	I_{OH} = −1.8mA	2.2	-	-	V
Input Leakage Current, High	I_{IH}	VDD = 3.6V VI = 3.6V	-	-	1	μA
Input Leakage Current, Low	$\|I_{IL}\|$	VDD = 3.6V VI = 3.6V	-	-	1	μA
Power Supply Current	I_{DD}	Fsclk = 0MHz	-	-	60	μA
		Fsclk = 1MHz,idle	-	-	180	
		Fsclk = 4MHz,idle	-	-	600	
		Fsclk = 32MHz,idle	-	-	4800	

Table 5 FBC0409 DC_2. Characteristics

Parameter	Symbol	VDD=5V±10% −40℃≤Ta≤85℃	Min.	Typical	Max.	Units
Input Voltage, High	V_{IH}	(1)	3.5	-	-	V
		(2)	2.7	3.4	4.1	
Input Voltage, Low	V_{IL}	(1)	-	-	1.5	V
		(2)	1.3	1.6	1.8	
Output Voltage, Low	V_{OL}	I_{OL} = 3mA	-	-	0.4	V
		I_{OL} = 15mA	-	-	1	

Output Voltage, High	V_{OH}	I_{OH} = −3mA	3.7	-	-	V
Input Leakage Current, High	I_{IH}	VDD = 3.6V VI = 3.6V	-	-	1	μ A
Input Leakage Current, Low	$\|I_{IL}\|$	VDD = 3.6V VI = 3.6V	-	-	1	μ A

Cautions:

(1) Input signal: PB_WR, PB_RD, PBI_INT_N, PB_DATA[7:0]

(2) Input signal: SCLK, NCLK, RST_N, RX_FFD, PB_ADDR[11:0], PB_RAMCS_N and PB_REGCS_N are Schmitt.

Table 6 FBC0409 A.C. Characteristics

Description	Symbol	Figure	Min.	Max.	Unit
SCLK high level width	Tpwh	5	10	Tcyc - 10	ns
SCLK low level width	Tpwl	5	10	Tcyc - 10	ns
SCLK frequence	Fsclk	5	1	32	MHz
NCLK high level width	Tpwh	5	75	Tcyc – 75	ns
NCLK low level width	Tpwl	5	75	Tcyc - 75	ns
NCLK frequence	Fnclk	5	1	4	ns
TX_FFD to TXEN delay	Tenst	6	0	±30	ns
Last half bit time	Tenfn	7	-	16u±30ns	-
TX_FFD jitter	Tjt	8	0	±20	ns
Register write pulse width	Tpwwr1	9	64	-	ns
Register write pulse width	Tpwrd1	9	64	-	ns
Register address setup time	Tas1	9,10	16	-	ns
Register address hold time	Tah1	9,10	16	-	ns
Register chipselect setup time	Tcss1	9,10	16	-	ns
Register chipselect hold time	Tcsh1	9,10	16	-	ns
Register write data setup time	Twds1	9	32		ns
Register write data hold time	Twdh1	9	16		ns
Register read data delay time	Trds1	10	-	40	ns
Register read data delay time	Trdh1	10	20	-	ns
Register Rdy setup time	Tws1	9,10	-	25	ns
Register Rdy assert time	Twh1	9,10	-	4	Tcyc
Ram write pulse width	Tpwwr2	9	128	-	ns
Ram write pulse width	Tpwrd2	9	128		ns
Ram address setup time	Tas2	9,10	16	-	ns
Ram address hold time	Tah2	9,10	16	-	ns

Ram chipselect setup time	Tcss2	9,10	16	-	ns
Ram chipselect hold time	Tcsh2	9,10	16	-	ns
Ram write data setup time	Twds2	9	32	-	ns
Ram write data hold time	Twdh2	9	16	-	ns
Ram read data delay time	Trds2	10	-	80	ns
Ram read data delay time	Trdh2	10	20	-	ns
Ram Rdy setup time	Tws2	9,10	-	25	ns
Ram Rdy assert time	Twh2	9,10	-	4	Tcyc

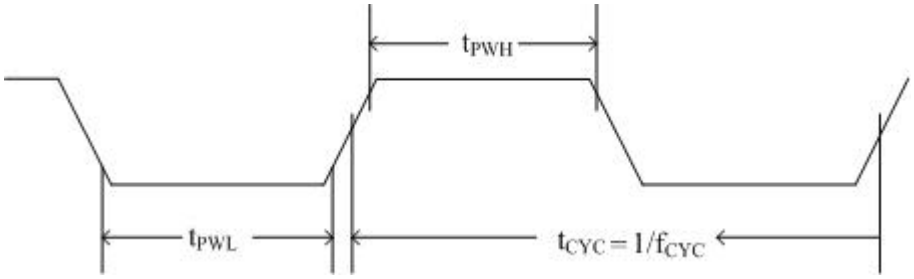

Figure 5 Clock Timing

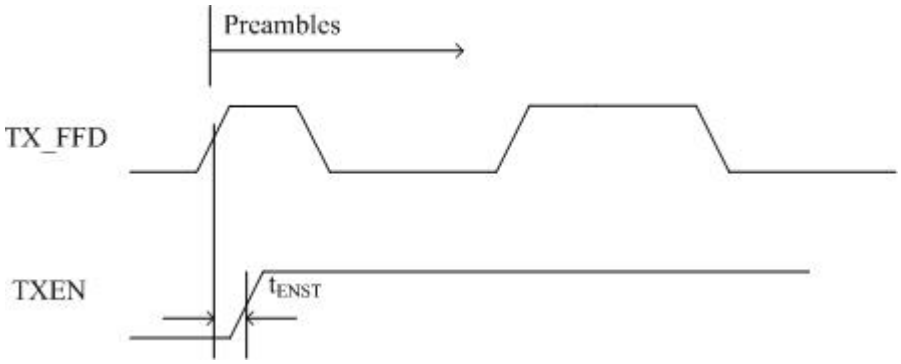

Figure 6 TX_FFD and TXEN Timing

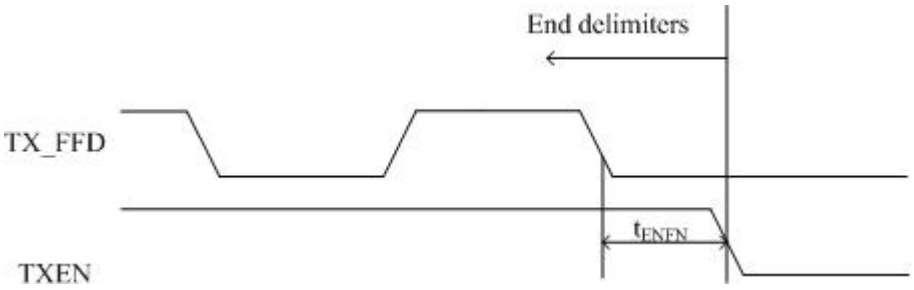

Figure 7 TX_FFD and TXEN Timing

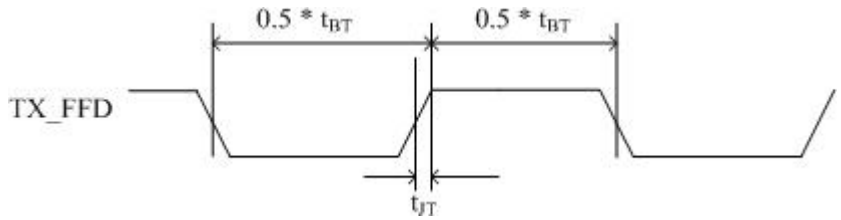

Figure 8 TX_FFD Timing

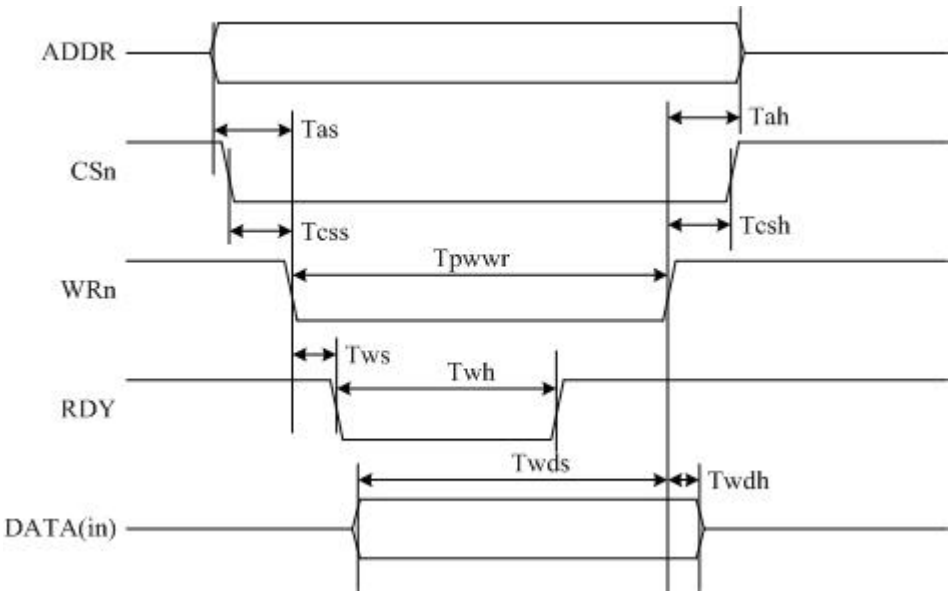

Figure 9 Write Operation Timing (include RAM and Register)

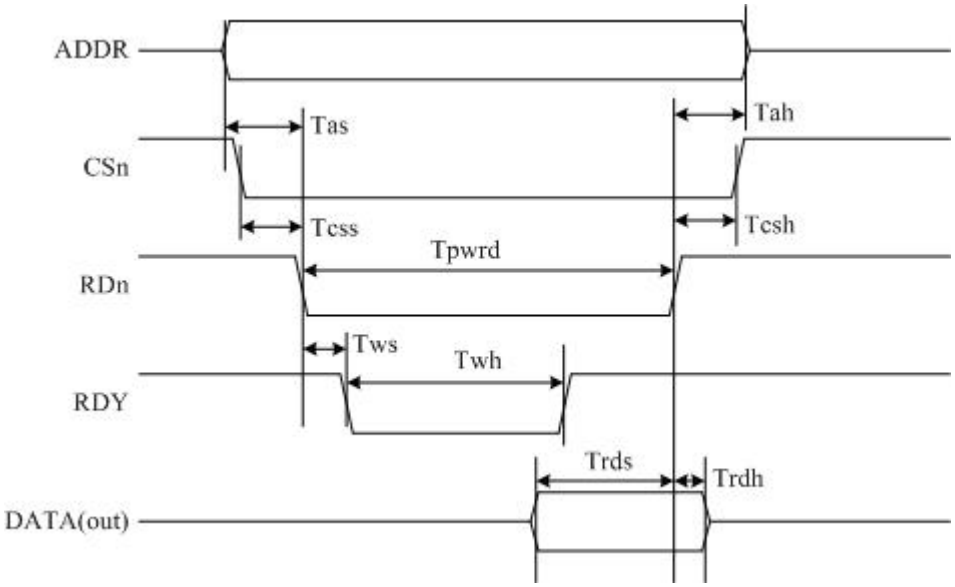

Figure 10 Read Operation Timing (include RAM and Register)

Package information

FBC0409 is TQFP44 package.

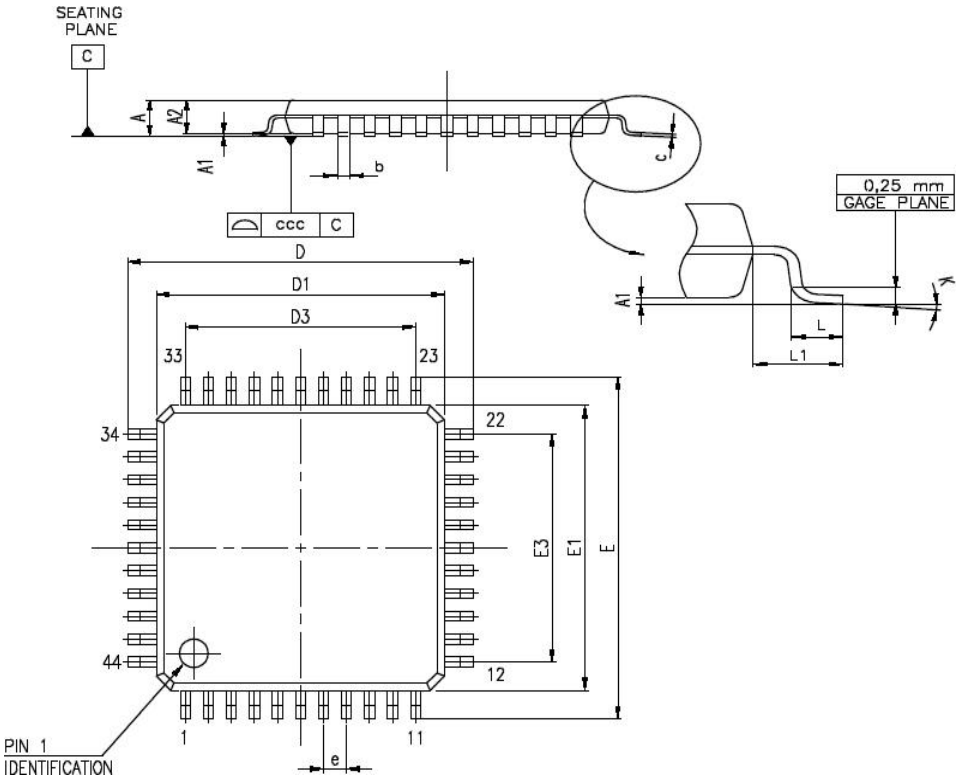

Figure 11 Package Diagram

Table 7 Packages Information

DIMENSIONS						
REF.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.6			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
B	0.30	0.37	0.45	0.012	0.015	0.018
C	0.09		0.20	0.004		0.008
D	11.80	12.00	12.20	0.465	0.472	0.480
D1	9.80	10.00	10.20	0.386	0.394	0.402
D3		8.00			0.315	
E	11.80	12.00	12.20	0.465	0.472	0.480
E1	9.80	10.00	10.20	0.386	0.394	0.402
E3		8.00			0.315	
e		0.80			0.031	
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
K	0°	3.5°	7°	0°	3.5°	7°

MICROCYBER

YOUR FIELDBUS EXPERT

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